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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,069	07/23/1999	PETER WOHL	SNSY-A1998-0	3639

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ART UNIT	**PAPER NUMBER**
2123	8

DATE MAILED: 03/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/360,069	WOHL ET AL.	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION: Non-Final (first office action after RCE)

Introduction

1. Title is: METHOD AND SYSTEM FOR GENERATING AN ATPG MODEL OF A MEMORY FROM BEHAVIORAL DESCRIPTIONS
2. First named inventor is: WOHL
3. Claims 1 (twice amended), 2, 3 (amended), and 4-36 have been submitted, examined, and rejected.
4. This is the first office action after Applicant's RCE received 1/23/03.

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5. **Cheng** refers to Gate-Level Test Generation for Sequential Circuits, by Kwang-Ting Cheng, ACM Transactions on Design Automation of Electronic Systems, Vol. 1, No. 4, October 1996, Pages 405-442.
6. **Beausang'771** refers to US Patent 5,696,771.
7. **Microsoft Computer Dictionary** refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.

Drawings-draftperson objection

8. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Specifically, see the previously sent Form 948, Notice of Draftperson's Drawing Patent Review which objects to the drawings.

Applicant's Request for Continued Examination

9. OBJECTION TO FORM OF AMENDMENTS.
10. Amendments page 2. The clean amended version of claim 1 states "1. (Amended)", but apparently should read "1. (Twice Amended)". The Examiner has corrected this minor clerical error in the amendments.
11. The amendments are accepted without other objection because they do not introduce new matter.
12. DEFINITIONS

13. Remarks page 3. Applicant persuasively distinguishes "a memory" from "a computer system memory".

14. Applicant asserts that **"a memory"** generally "is used to describe the logical representation of a **memory cell and/or device** being designed and tested...". The use of the term "and/or" is ambiguous regarding whether an adjective (memory) apply only the first noun (cell) or to both nouns (cell and device). The Examiner interprets this definition to mean "logical representation of a **memory cell or a memory device**...". See MPEP 2111.01 regarding claim interpretation using plain meaning of words.

15. Remarks page 3. Applicant persuasively asserts that **"a computer system memory"** generally "is used to describe the physical location for storing the logical representation in the computer system".

16. The Examiner adopts Applicant's above two definitions for use throughout this office action.

17. Remarks page 4. Applicant unpersuasively asserts that "a memory" is an element of claim 1 (twice amended). Note that there are three memory models that are elements in claim 1 (twice amended): a simulation model of a memory, a simplified behavioral model of a memory, and a structural model of a memory. It is possible that the Applicant intends "a memory" to refer to an original logical representation which was used to create the simulation model of a memory, but this intent is not clear from Applicant's definition of "a memory". If this is the Applicant's intent, then the original logical representation is not an element of claim 1 (twice amended). Note that the simulation model of a memory already exists in step A, and this simulation model of a memory appears to be the starting point of the method claim.

18. COLLECTIVE FUNCTIONAL LIMITATIONS

19. Remarks page 4. Applicant conditionally agrees to discuss functional limitations collectively for convenience, but reserves the right to explicitly address individual elements and functions if necessary. The Examiner agrees that this is an efficient way to expedite prosecution.

20. Remarks page 5-10. Applicant discusses the 35 USC 102 and 103 rejections. These remarks will be explicitly addressed below in the rejections as appropriate.

Claim Rejections - 35 USC § 112-Second Paragraph-indefinite claims

21. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

22. **Claim 1 (twice amended) rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

23. Claim 1 (twice amended), step B, states **"re-describing said memory".** This term is vague and indefinite regarding which logical representation of a memory cell or a memory device is being "re-described". The Examiner interprets this term to mean "re-describing said simulation model of a memory". Note that there are three memory models that are elements in claim 1 (twice amended): a simulation model of a memory, a simplified behavioral model of a memory, and a structural model of a memory. See above discussion regarding definitions, and see below discussion for detailed interpretation.

Claim Interpretation

24. The claim language is interpreted in light of the specification. Limitations from the specification must not be imported into the claims, but definitions from the specification must be imported into the claims.

25. The Examiner interprets this term to mean "re-describing said simulation model of a memory". This interpretation is made in view of Specification FIG 3 elements 301 and 330. Note that the "simulation model of said memory" appears to be the earliest model of a memory discussed in claim 1 (twice amended).

26. The following summary of the four steps of method claim 1 (twice amended) illustrates this interpretation using three memory models (simulation, simplified behavioral, and structural):

27. step A: a **simulation model** (behavioral HDL) is accessed.

28. step B: said simulation model is re-described to create a **simplified behavioral model** (using proper subset of behavioral HDL).

29. step C: said simplified behavioral model is translated into a **structural model** (plurality of ATPG memory primitives).

30. step D: said structural model is stored.

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

33. Claims 1 (twice amended), 2, 3 (amended), and 4-36 are rejected under 35 U.S.C. 103(a) as being unpatentable.

34. Claim 1 (twice amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of MPEP 2144.04(II)(A) Routine Expedient of omission of an element and its function, and Official Notice, and Cheng.

35. Claim 1 (twice amended) is an independent method claim with 4 steps, labeled A-D by the Examiner.

36. A-**accessing a simulation model of said memory, from a simulation library stored in a computer system memory, wherein said simulation model is described in a behavioral hardware description language** is disclosed by Beausang'771 at FIG 8 element 605 "HDL DESCRIPTION". Note that HDL stands for "hardware description language". The Examiner hereby takes official notice that it is common knowledge to create simulation models of memories using hardware description languages (such as VHDL or Verilog), and to store these models in a simulation library in a computer system memory, and to access this simulation model.

37. Applicant has the right to traverse this official notice according to MPEP § 2144.03: "if applicant traverses such an assertion, the examiner should cite a reference in support of his or her position". However, please note that MPEP § 2144.03 also states "See also In re Boon, 439 F.2d 724, 169 USPQ 231 (CCPA 1971) (a challenge to the taking of judicial notice must

contain adequate information or argument to create on its face a reasonable doubt regarding the circumstances justifying the judicial notice)". Specifically, please note that In re Boon states, at 169 USPQ 231, page 234, that "as we held in Ahlert, an applicant must be given the opportunity to challenge either the correctness of the fact asserted or the notoriety or repute of the reference cited in support of the assertion. We did not mean to imply by this statement that a bald challenge, with nothing more would be all that was needed", and "require that a challenge to judicial notice by the board contain adequate information or argument so that on its face it creates a reasonable doubt regarding the circumstances justifying the judicial notice." Additionally, please note that 37 CFR 1.671(c)(3) states "Judicial notice means official notice". Therefore, in view of MPEP § 2144.03 and In re Boon and 37 CFR 1.671(c)(3), the Applicant should note that a mere "bald challenge, with nothing more" to the above official notice will be given very little weight.

38. C-**translating, automatically and under control of a computer system, said simplified behavioral model of said memory into said structural model of said memory, wherein said structural model comprises a plurality of ATPG memory primitives** is disclosed by Beausang`771 at FIG 8

39. element 605 "HDL DESCRIPTION" and element 615 "COMPILE..." and element 655 "ATPG AND FORMAT".

40. **Remarks page 7.** Applicant persuasively asserts that Beausang'771 contains elements and functions not present in claim 1 (twice amended). However,

41. note that Beausang'771 is being used as prior art in a 35 USC 103 rejection against a claim that contains the preamble transitional phrase of "comprising the steps of".

42. Beausang`771 does not explicitly disclose the remaining limitations.

43. B-**generating a simplified behavioral model of said memory by re-describing said memory with a predefined proper subset of said behavioral hardware description language** is Routine Expedient. MPEP 2144.04(II)(A) states that "Omission of an Element and Its Function Is Obvious If the Function of the Element Is Not Desired". Here, for example, a proper subset may be created by eliminating timing information when "not desired or required" according to MPEP 2144.04(II)(A). As a second example, a second

proper subset may be created by eliminating layout information when "not desired or required" according to 2144.04(II)(A). Thus, this second step is disclosed by legal precedent.

44. **Remarks page 4.** Applicant unpersuasively distinguishes *Ex parte Wu,* 10 USPQ2d 2031, 2032 (Bd. Pat. App. & Inter. 1989). The Applicant appears to mischaracterize this case. The MPEP states "The Board affirmed the rejection, holding that it would have been obvious to omit the polybasic acid salts of the primary reference where the function attributed to such salt is not desired or required, such as in compositions for providing corrosion

45. resistance in environments which do not encounter fresh water". Similarly, in this claim, eliminating timing information when timing information is not needed is also obvious.

46. Additionally, *In re Larson,* 340 F.2d 965, 144 USPQ 347, 350 (CCPA 1965) states "If this additional features (sic) is not desired, it would seem a matter of obvious choice to eliminate it and the function it serves".

47. Further, note that MPEP 2144.04(II)(B) states "the omission of an element and retention of its function is an indicia of nonobviousness". However, the function is not retained in this claim, so there is no indicia of nonobviousness.

48. D-**storing said structural model in said computer system memory** is disclosed by Official Notice that it is common knowledge in the art to store structural models in computer system memories.

49. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Routine Expedient and Official Notice and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a proper subset (Routine Expedient) to create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407. Further, one of ordinary skill in the art would have been motivated to store these models in a simulation library in a computer system memory in order to easily access these models for various computer simulations to test the circuit design.

50. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of MPEP 2144.04(II)(A) Routine Expedient of omission of an element and its function, and Official Notice, and Cheng.

51. Claim 2 depends from claim 1 (twice amended), with one additional limitation.

52. Beausang'771 does not expressly disclose the additional limitation.

53. **simplified behavioral model excludes timing information** is disclosed by Routine Expedient, as discussed above in Claim 1 (twice amended).

54. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Routine Expedient and Official Notice and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a proper subset (Routine Expedient) to create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407. Further, one of ordinary skill in the art would have been motivated to store these models in a simulation library in a computer system memory in order to easily access these models for various computer simulations to test the circuit design.

55. **Applicant Remarks page 8, regarding claim 2 and claim 3 (amended).**

56. Applicant persuasively asserts that Cheng's structural models do appear to contain timing and/or layout information, because Cheng explicitly discloses "ignoring" delays. Applicant proposes that Cheng's delays result from different signal propagation paths, and that Cheng retains and utilizes timing and/or layout information. The Examiner is not certain exactly which "circuit delays" Cheng is ignoring. Cheng at page 406 states "We focus on the methods that are based on gate-level circuit models". Thus, these delays appear to be at least dependent upon the timing and/or layout information. Therefore, Cheng at page 407 appears to retain certain information, but ignores this information (or at least the delays that results from it) during a "potential test".

57. Please note that Cheng is not used in this rejection for disclosing the specific limitation of excluding timing and/or layout information from a structural model. Cheng is used only for motivation. Cheng specifically discloses performing some tests using ATPG methods while ignoring delays. Thus, Cheng serves as motivation for combining the Routine Expedient of

omission of an element and its function (delays or timing/layout related information) with the "HDL" and "ATPG" of Beausung'771. In other words, Cheng discloses that it is well known in the art that delays or timing/layout related information is sometimes not desired. Note that *In re Larson,* 340 F.2d 965, 144 USPQ 347, 350 (CCPA 1965) states "If this additional features (sic) is not desired, it would seem a matter of obvious choice to eliminate it and the function it serves".

58. Claim 3 (amended) is rejected under 35 U.S.C. 103(a) as being unpatentable over Beausang'771 in view of MPEP 2144.04(II)(A) Routine Expedient of omission of an element and its function, and Official Notice, and Cheng.

59. Claim 3 depends from claim 2, with one additional limitation.

60. Beausang'771 does not expressly disclose the additional limitation.

61. **said simplified behavioral model excludes physical layout information contained in said simulation model of said memory** is disclosed by Routine Expedient, as discussed above in Claim 1 (twice amended).

62. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Routine Expedient and Official Notice and Cheng to modify Beausang'771. One of ordinary skill in the art would have been motivated to use a proper subset (Routine Expedient) to create simulation models of memories using hardware description languages (such as VHDL or Verilog) in order to simulate integrated circuits while "ignoring the circuit delays" according to Cheng at Page 407. Further, one of ordinary skill in the art would have been motivated to store these models in a simulation library in a computer system memory in order to easily access these models for various computer simulations to test the circuit design.

63. Claims 4-12 all depend from Claim 1 (twice amended), and are rejected for the same reasons as Claim 1 (twice amended) above, in addition to the reasons previously stated in the previous Office Action, mailed 5/9/02. There have been no amendments to claims 4-12. The Applicant's only specific discussion regarding the limitations of claims 4-12 is presented below.

64. Applicant Remarks page 9, regarding claims 4-8.

65. Applicant unpersuasively asserts that Beausang'771 does not explicitly teach what a logical primitive represents. And Applicant unpersuasively distinguishes the present claims from Beausan'771, stating that "an ATPG memory primitive according to the present invention comprises a plurality of other primitives (e.g., memory primitive, address bus primitive, read port primitive, etc.)".

66. Beausang'771 must be interpreted in the light of what one of ordinary skill in the art would know. Microsoft Computer Dictionary defines logical as "logical" as "Based on true and false alternatives as opposed to arithmetic calculation of numeric values... Boolean algebra", and defines "primitive" as "In programming, a fundamental element in a language that can be used to create larger procedures that do the work a programmer wants". Thus, Beausang'771 broadly teaches logical primitives, including memory primitives and including pluralities of primitives.

67. Claims 13-24 are "computer readable medium" claims with the same limitations as "method" Claims 1-12, and therefore are rejected for the same reasons. Note that claim 13 is analogous to claim 1, but has not yet been "twice amended" like claim 1 has been. Similarly, claim 15 is analogous to claim 3, but has not yet been "amended" like claim 3 has been. The Examiner believes that Applicant's intent is that the "computer readable medium" claims should mirror the limitations of the "method" claims.

68. Claims 25-36 are "computer controlled electronic design automation systems" (apparatus) claims with the same limitations as "method" Claims 1-12 and therefore are rejected for the same reasons. Note that claim 25 is analogous to claim 1, but has not yet been "twice amended" like claim 1 has been. Similarly, claim 27 is analogous to claim 3, but has not yet been "amended" like claim 3 has been. The Examiner believes that Applicant's intent is that the "computer controlled electronic design automation system" (apparatus) claims should mirror the limitations of the "method" claims.

Communication

69. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM.

70. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

71. (703) 746-7238 --- for communications after a Final Rejection has been made;

72. (703) 746-7239 --- for other official communications; and

73. (703) 746-7240 --- for non-official or draft communications.

74. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

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